AMENDMENTS TO THE CLAIMS

1. (Original) IC-circuit construction whereby the circuit on the IC is partitioned into power consuming sub-circuits (1,6) which each has a power supply, and whereby the sub-circuits (1,6) are connected in series.

2. (Original) IC-circuit as claimed in claim 1 whereby a control-circuit (4) is provided in order to balance the voltage drops across the power consuming sub-circuits (1,6) whereby constant voltage-drops over the sub-circuits (1,6) are maintained.

3. (Original) IC-circuit as claimed in claim 1 or claim 2 whereby the sub-circuits (1,6) are digital or analog or mixed signal circuits.

4. (Original) IC circuit as claimed in claim 1 whereby the sub-circuits (1,6) are located on each their chip.

5. (Currently Amended) IC circuit as claimed in ~~any of the above claims~~ claim 1, whereby two sub-circuits (1,6) are series-connected such that the ground voltage level (VHH) in the power supply of the first sub-circuit (1) is used as the supply voltage level in the second sub-circuit (6).

6. (Currently Amended) IC circuit as claimed in claim ~~5~~ 2, whereby the control circuit comprises a first buffer capacitor (10) coupled in parallel over the supply voltage level (VBB) and ground voltage level (VHH) of the first sub-circuit (1) and a second buffer capacitor (11) coupled in parallel over the supply voltage level (VHH) and the ground voltage level (GND) of the second sub-circuit (6), and whereby means for maintaining a uniform voltage drop over the first (10) and the second (11) buffer capacitor comprises at least one bucket capacitor (20,21,22) which is alternately coupled in parallel over the first (10) and the second (11) buffer capacitor through a switching system controlled by a signal that toggles at a sufficient rate.

7. (Original) IC circuit as claimed in claim 6, whereby there are two bucket capacitors (21,22) that get switched at the same time such as to alternately couple to the first and the second buffer capacitor respectively.

8. (Original) IC circuit as claimed in claim 6 or 7, whereby the switches (25,28,35,36,37,38) for alternately coupling the bucket capacitors (20,21,22) are controlled by a free-running oscillator (17), a clock, or some other suitable signal of periodic or nonperodic nature.

9. (Original) IC circuit as claimed in claim 6, whereby the means for maintaining a uniform voltage drop over the first (10) and the second (11) buffer capacitor comprises a voltage reference and a comparator (12), which generates control signals for voltage control means.

10. (Original) IC circuit as claimed in claim 2 whereby the control circuit (4) is designed such as to maintain different voltage drops across the sub-circuits (1,6).